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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,278	10/11/2003	Raymond G. Beausoleil	200311663-1	3329

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CONNELLY CUSHWA, MICHELLE R	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,278	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Michelle R. Connelly-Cushwa	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,17-19,40-42,44-46,48,49 and 51-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-19 and 40* is/are allowed.

6)☒ Claim(s) *1,2,5,6 and 51-62* is/are rejected.

7)☒ Claim(s) *3,4,41,42,44-46,48 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2003 and 14 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's Amendment filed September 11, 2006 has been fully considered and entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6, 59 and 60-62 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamanaka (US 5,202,567).

Regarding claim 1; Hamanaka discloses an interconnect system comprising:

- a first circuit unit (11; see Figures 1-3) containing a first electronic circuit (4) and a plurality of modulators (spatial-light modulator array, SLM, 32), wherein:
    - the first electronic circuit produces a plurality of electrical output signals; and
    - each modulator is controlled by a corresponding one of the electrical output signals and is capable of modulating a corresponding component of a first optical signal (A') output from the first circuit unit (see column 4, lines 42-49); and

- a second circuit unit (12) containing a second electronic circuit and a plurality of detectors (sensor array, 31), wherein:
    - the second electronic circuit processes a plurality of electrical input signals; and
    - each detector is capable of detecting modulation of a corresponding one of the components of the first optical signal to extract a corresponding one of the input signals (see column 4, lines 38-49).

Regarding claim 2; the second circuit unit further comprises a second plurality of modulators (32), wherein each modulator in the second circuit unit is capable of modulating a corresponding component of a second optical signal; and the first circuit unit further comprises a second plurality of detectors (31), wherein each detector in the first circuit unit is capable of detecting modulation of a corresponding one of the components of the second optical signal to extract a corresponding electrical signal.

Regarding claim 5; the first circuit unit (11) is integrated on a first chip and the second circuit unit (12) is integrated on a second chip.

Regarding claim 6; a first light source (S in Figure 3) that is external to the first chip (11) provides the first optical signal (A) to the first circuit unit.

Regarding claim 59; the first circuit unit (11) and the second circuit unit (12) are integrated into a single device (see Figure 3).

Regarding claim 60; the first circuit unit (11) is a first chip, the second circuit unit (12) is a second chip, and the first and second chips (10 in Figure 4) may be mounted on a substrate (motherboard, 20, in Figure 4).

Regarding claim 61; a source of light (60) may be mounted on the substrate (20).

Regarding claim 62; the first and second circuit units are integrated into a chip (see Figure 3; the chip is formed by stacking each of the circuit units) and the first optical signal propagates from the first circuit unit to the second circuit unit within the chip.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 51-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 2002/0009277 A1).

Regarding claim 51-56; Noda et al. discloses an interface of an integrated circuit (see Figure 2), comprising:

- a waveguide (line defect, 12, forms a waveguide) for an optical signal (23) that includes a plurality of frequency components ($\lambda 1$, $\lambda 2$,... λi, λj);
- a plurality of resonators (point defects, 21 and 22) adjacent to the waveguide (line defect, 12), wherein the resonators respectively

correspond to frequency components, and each of the resonators provides a path for a corresponding frequency component; and

- a plurality of electrical elements (photodiodes, 45, 46 and 47; see Figure 8) respectively associated with the resonators;
- wherein the electrical elements (photodiodes) implement transformations between the plurality of frequency components and a plurality of electrical signals;
- wherein the interface comprises a photonic bandgap crystal.

Noda et al. does not explicitly state that the interface is of an electronic integrated circuit or that the electrical signals are processed in an electronic integrated circuit. However, the photodiodes do convert the optical signals into electrical signals, and it is well known in the art that electronic circuits are required to process electronic signals. Therefore, one of ordinary skill in the art would have found it obvious to use the interface disclosed by Noda as an interface of an electronic integrated circuit by connecting the outputs of the photodiodes to an electronic integrated circuit to process the electrical signal output of the photodiodes to obtain the desired information from the signals or to use the output electrical signals for a desired utility.

Regarding claim 57; Noda et al. further discloses that each of the resonators (point defects) may optionally feed the corresponding frequency components into the waveguide (see paragraph [0059]) in order to form a multiplexer.

Regarding claim 58; Noda et al. discloses all of the limitations of claim 58 as applied above, except for each of the electronic elements comprising a modulator that

modulates the frequency components that the associated resonator feeds into the waveguide. Pearsall teaches that electronic elements can be provided adjacent to point defects in photonic crystals to modulate the frequency response of the point defect. One of ordinary skill in the art would have found it obvious to provided electronic elements adjacent to the point defects in the invention of Noda et al. to modulate the frequency response of the point defects to thereby fine-tune the multiplexed and/or demultiplexed wavelengths as desired.

Allowable Subject Matter

Claims 3, 4, 41, 42, 44-46, 48 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 17-19 and 40 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art cited on attached form PTO-892 is the most relevant prior art known, however, the invention of claims 3, 4, 17-19, 40-42, 44-46, 48 and 49 distinguishes over the prior art of record because none of the references either alone or in combination disclose or render obvious:

- a system as defined in claim 3, wherein the first circuit unit comprises a photonic bandgap crystal, wherein each of the modulators comprises a defect within the photonic bandgap crystal and an electrode adjacent the defect, wherein the defect acts as a resonator for the corresponding component of the first optical signal and has a property

that varies with a voltage applied to the electrode in combination with the limitations of base claim 1;

- a system as defined in claim 4, wherein each of the detectors comprises a photodiode at a corresponding defect within a photonic bandgap crystal, wherein the defect acts as a resonator for the corresponding component of the first optical signal in combination with the limitations of base claim 1;
- an interface as defined in claim 17 comprising a first plurality of point defects within the photonic bandgap crystal, a plurality of electrical elements respectively adjacent to the first plurality of point defects, a second plurality of point defects, and a plurality of modulators respectively adjacent to the second plurality, wherein the modulators respectively respond to electrical output signal of the electronic integrated circuit to modulate optical signals respectively having the wavelengths that are resonant with the adjacent point defects in combination with the other limitations of claim 17;
- a system as defined in claim 44, wherein the first circuit unit comprises a photonic bandgap crystal containing a plurality of defects, wherein each of the defects acts as a resonator for a different one of the components of the first optical signal, and a material in each of the defects has a refractive index that depends on an electric field in the material; and a plurality of electrodes respectively adjacent to the

plurality of defects, wherein the electronic outputs signal are respectively applied to the electrodes to change the electric fields in the respective defects in combination with the limitations of base claim 1;

- a system as defined in claim 46, wherein the first circuit unit comprises a first waveguide for input of light, a plurality of drop filters positioned to respectively extract and separated the plurality of frequency components, wherein the plurality of modulators are associated with the plurality of drop filters, and a second waveguide into which the frequency components form the modulators are directed in combination with the other limitations of claim 46 and the limitations of base claim 1;
- a system as defined in claim 48, wherein the second circuit unit further comprises a photonic bandgap crystal containing a plurality of defects, wherein each of the defects acts as a drop filter for a different wavelength of light; and the plurality of detectors are respectively associated with the plurality of defects, wherein each detector generates an electrical signal that indicates a modulation of a light signal extracted by the associated defect in combination with the limitations of base claim 1; or
- a system as defined in claim 49, wherein the second circuit unit comprises a waveguide for the first optical signal, and a plurality of

drop filters positioned to respectively extract the components of the first optical signal, wherein the plurality of detectors are associated with the plurality of drop filters in combination with the other limitations of claim 49 and the limitations of base claim 1.

Claims 41 and 42 depend from claim 3; claims 18, 19 and 40 depend from claim 17; claim 45 depends from claim 44.

Hence, there is no reason or motivation for one of ordinary skill in the art to use the prior art of record to make the invention of claims 3, 4, 17-19, 40-42, 44-46, 48 and 49.

Response to Arguments

Applicant's arguments with respect to claims 1, 2, 5, 6 and 59-62 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 51-58 have been fully considered but they are not persuasive. Applicant states that Noda discloses optical demultiplexing and conversion of optical signals to electrical signals, but that Noda fails to suggest use of such in an interface of an electronic integrated circuit. The photodiodes disclosed by Noda, however, output electrical signals. Electrical signals are inherently used to interface with electronic integrated circuits, since such circuits are required to utilize the electrical signals and/or to further process the electrical signals.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning the merits of this communication should be directed to Examiner Michelle R. Connelly-Cushwa at telephone number (571) 272-2345. The examiner can normally be reached 9:00 AM to 7:00 PM, Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney B. Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general or clerical nature should be directed to the Technology Center 2800 receptionist at telephone number (571) 272-1562.

Michelle R. Connelly-Cushwa
Michelle R. Connelly-Cushwa
Patent Examiner
December 6, 2006